What is claimed is:

1. A method of making a bump on a substrate comprising:

providing a substrate having a bond pad thereon;

depositing an electrically conductive redistribution trace over the substrate, and wherein the electrically conductive redistribution trace is in electrical contact with the bond pad and extends a distance horizontally from the bond pad;

selectively depositing a removable buffer material onto the electrically conductive redistribution trace at a location spaced a distance horizontally from the bond pad;

depositing a stress buffer layer over the substrate and encapsulating the removable buffer material;

removing a portion of the stress buffer layer to expose the removable buffer material;

removing the removable buffer material to provide an opening in the stress buffer layer down to the electrically conductive redistribution trace;

depositing an electrically conductive material into the opening in the stress buffer layer and overlying the electrically conductive redistribution trace; and

reflowing the electrically conductive material to provide a bump on the substrate.

2. A method as set forth in claim 1 further comprising depositing an under bump metallurgy structure over the substrate and in electrical contact with the bond pad prior to depositing the electrically conductive redistribution trace.

3. A method as set forth in claim 2 wherein the under bump metallurgy includes a plurality of layers.

4. A method as set forth in claim 2 wherein the under bump metallurgy includes a first comprising titanium and second layer comprising copper.

5. A method as set forth in claim 1 wherein the stress buffer layer comprises benzocyclobutene.

6. A method as set forth in claim 1 wherein the stress buffer layer comprises a polyimide.

7. A method as set forth in claim 1 wherein the stress buffer layer comprises a modified polyimide prepreg.

8. A method as set forth in claim 1 wherein the electrically conductive material comprises solder.

9. A method as set forth in claim 1 wherein the electrically conductive redistribution trace comprises copper.

10. A method as set forth in claim 1 further comprising the step of depositing at least a first seed layer into the opening in the stress buffer layer prior to depositing the electrically conductive material.

11. A method as set forth in claim 10 wherein the first seed layer comprises copper.

12. A method as set forth in claim 1 further comprising a passivation layer overlying the substrate and having an opening formed in the passivation layer to expose a portion of the bond pad.

13. A method as set forth in claim as set forth in claim 1 wherein the act of removing a portion of the stress buffer layer comprises chemical mechanical planarizing the stress buffer layer to expose the removable buffer material.

14. A method as set forth in claim 1 wherein the removable buffer material comprises a photoresist.

15. A method as set forth in claim 14 wherein the act of removing the removable buffer material comprises wet etching the photoresist.

16. A method as set forth in claim 1 wherein removable buffer material comprises a dry film photoresist.

17. A method as set forth in claim 16 wherein the act of removing the removable buffer material comprises wet etching the dry film photoresist.

18. A method of making a bump on a semiconductor wafer comprising:

providing a semiconductor wafer having a contact pad and having an upper passivation layer and an opening formed in the passivation layer exposing a portion of the contact pad;

depositing an under bump metallurgy structure over the upper passivation layer and the contact pad;

depositing an electrically conductive redistribution trace over the under bump metallurgy structure;

depositing, patterning and developing a photoresist layer to provide a first patterned photoresist layer selectively protecting a portion of the electrically conductive redistribution trace and the under bump metallurgy structure;

removing excess portions of the electrically conductive redistribution trace and the under bump metallurgy structure not protected by the first patterned photoresist layer;

removing the first patterned photoresist layer;

depositing, patterning and developing a second photoresist layer over the electrically conductive redistribution trace to provide a second patterned photoresist layer selectively positioned over the electrically conductive redistribution trace at location spaced a distance horizontally from the bond pad;

depositing a stress buffer layer over the semiconductor device encapsulating the second patterned photoresist layer;

chemical mechanical planarizing the stress buffer layer to expose the second patterned photoresist layer;

removing the second patterned photoresist layer to provide an opening in the stress buffer layer down to the electrically conductive redistribution trace;

depositing an electrically conductive material into the opening in the stress buffer layer; and

and reflowing the electrically conductive material to provide a bump on the semiconductor wafer.

19. A method as set forth in claim 18 further comprising the step of depositing at least a first seed layer into the opening in the stress buffer layer prior to the step of depositing electrically conductive material into the opening in the stress buffer layer.

20. A method as set forth in claim 18 wherein the step of removing the second patterned photoresist layer comprises wet etching the second patterned photoresist layer.